UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,528	02/07/2007	Hitoshi Tsuge	292022US2PCT	9466

22850 7590 09/09/2010

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/09/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/581,528	TSUGE, HITOSHI	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *69,70 and 72-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *69,70 and 72-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 August 2010 has been entered. Claims 69, 70 and 72-77 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 69, 70 and 72-77 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 69 and 70 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 69 was amended to recite "the gradation voltage which is supplied from said voltage generation section to said driving transistors, is applied so as to change gate voltages of said driving transistors in consideration of current/voltage characteristics of said driving transistors, respectively, such that the sum of currents flowing through said self-luminescent elements is a predetermined current value." To support this limitation the Applicant states that paragraphs [0324], [0331] and [0332] and Figures 12(a0 and 12(b) of the Applicant's published specification support this feature, however, these paragraphs merely disclose that the current/voltage characteristics of a single transistor can be changed, but there is nothing in there paragraphs detailing that the gradation voltage is applied to change the gate voltages of the driving transistors such that the sum of currents flowing through said self-luminescent elements is a predetermined current value as claimed in claim 69. Thus it appears that there is insufficient support for the amendments to the claim.

Claim 70 was amended to recite "the voltage which is supplied from said voltage generation section to said driving transistors, is applied so as to change gate voltages of said driving transistors according to temperature in consideration of current/voltage characteristics of said driving transistors, respectively." To support this limitation the

Applicant states that paragraph [0019] and Figure 10 of the Applicant's published specification support this feature, however, paragraph [0019] is referring to compensating for the temperature characteristic of the transistor 103 in Figure 10, which is not a driving transistor of a pixel as claimed in claim 70. Thus it appears that there is insufficient support for the amendments to the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 69, 70, 72, 73 and 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 2002/0105279) in view of Tsuruoka et al. (US 6,414,443) and further in view of Abe (US 2004/0041750).

Regarding claim 69, Kimura discloses a self-luminescent display apparatus comprising:

self-luminescent elements arranged in a pattern of a matrix (Figure 1, 101 is a pixel portion with a plurality of pixels 102 arranged in a matrix pattern with OLEDs 105

in each of the pixels (OLEDs are self-luminescent elements). See paragraphs [0050] and [0051]);

driving transistors, each of which controls a current supplied to each of said self-luminescent elements (Figure 4 shows driving TFT 111 which will be provided in each pixel as shown in Figure 1. See paragraphs [0059]-[0061].);

pixel circuits provided in association with each of said self-luminescent elements and each of said driving transistors (Figure 1, 102 and Figure 4. See paragraph [0059].); and

a voltage generation section to supply a gradation voltage, which is to correspond to a display grade, to said driving transistors (Figures 1 and 4, 106 and paragraphs [0052], [0059] and [0061] explain that the variable power supply 106 controls the OLED drive voltage of the OLED in each pixel meaning that it supplies a voltage which corresponds to a display grade as claimed, and as shown in the Figures, this voltage is applied to the driving transistors in each pixel.).

Kimura fails to explicitly teach wherein the gradation voltage is supplied from said voltage generation section to said driving transistors such that the sum of currents flowing through said self-luminescent elements is a predetermined current value.

Tsuruoka et al. disclose a self-luminescent display apparatus comprising:

a voltage generation section to supply a gradation voltage, which is to correspond to a display grade, to pixels of the display (Figure 4, 34. See column 5, lines 50-54.),

wherein the gradation voltage is supplied from said voltage generation section to said pixels such that the sum of currents flowing through said self-luminescent elements is a predetermined current value (Figure 3 and column 5, line 65 to column 6, line 37 and column 6, line 64 to column 7, line 2.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Tsuruoka et al. in the self-luminescent display apparatus taught by Kimura such that the sum of currents flowing through said self-luminescent elements is a predetermined current value in order to obtain enhanced display quality (Tsuruoka et al., column 6, lines 35-37).

Kimura and Tsuruoka et al. fail to each that the gradation voltage is applied so as to change gate voltages of said driving transistors in consideration of current/voltage characteristics of said driving transistors.

Abe discloses a self-luminescent display apparatus wherein a gradation voltage is applied so as to change gate voltages of said driving transistors in consideration of current/voltage characteristics of said driving transistors (Paragraphs [0070] and [0073]. See also claim 3.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Abe in the self-luminescent display apparatus taught by the combination of Kimura and Tsuruoka et al. in order to increase the image quality of the display apparatus (See Abe, paragraph [0008]).

Regarding claim 70, please refer to the rejection of claim 69, and furthermore Tsuruoka et al. also discloses where the voltage outputted from said voltage generating section is changed according to temperature (Figures 2B and 4 and column 5, line 24 to column 6, line 25).

Regarding claim 72, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Tsuruoka et al. also disclose wherein said voltage generation section adjusts the gradation voltage such that when the gradation voltage is supplied to said pixels, the sum of currents flowing through said self-luminescent elements is measured and adjusted to be the predetermined current value (Figure 3 and column 5, line 65 to column 6, line 37 and column 6, line 64 to column 7, line 2. [where in combination the gradation voltage would be supplied to the driving transistors]).

Regarding claim 73, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Kimura also discloses the apparatus further comprising:

an adjustor circuit to adjust the gradation voltage generated by said voltage generation section (Figure 4, current circuit 108 is the "adjuster circuit" as claimed since it adjusts the voltage generated by variable power supply 106.), and

a memory unit to store a voltage value set by said adjustor circuit (Figure 4, capacitor 112 is a memory unit which will store the voltage.).

Regarding claim 75, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Tsuruoka et al. also disclose the apparatus further comprising:

a temperature compensation unit to generate a signal inputted to said voltage generation section according to the change of ambient temperature, wherein the gradation voltage outputted from said voltage generation section is changed by the signal inputted from said temperature compensation unit, thereby to compensate for a temperature characteristic of the currents flowing through said self-luminescent elements (Figure 2b and 4, 35 and column 5, line 38 to column 6, line 24.).

Regarding claim 76, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Kimura also discloses wherein said voltage generation section comprises at least one predetermined circuit including said driving transistor and a storage capacity, disposed in said pixel circuit, and the gradation voltage is generated based on a gate voltage or drain voltage of said driving transistor (Figure 4 shows that driving transistor 111 and capacitor 112 are part of the "voltage generation section" since they receive the voltage from the variable power supply and then generate the driving of the OLED 105. See paragraphs [0059]-[0061].).

Regarding claim 77, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 76.

Kimura also discloses wherein at least two predetermined circuits including said driving transistor and a storage capacity (Figures 1 and 4), respectively, are provided, and one of said predetermined circuits is selected and used as said voltage generation section (Figures 1 and 4, where one of the circuits will be selected in the first row when the gate signal is high, and then the pixel circuit will be used to generate the voltage as shown in Figure 4. Thus one of the circuits will be selected and used as said voltage generation section.).

7. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 2002/0105279) in view of Tsuruoka et al. (US 6,414,443) and further in view of Abe (US 2004/0041750) and Kasai (US 6,989,826).

Regarding claim 74, Kimura, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Kimura, Tsuruoka et al. and Abe fail to teach wherein the display grade corresponds to a grade of black display

Kasai discloses a self-luminescent display apparatus wherein a display grade applied to the pixels corresponds to a grade of black display (Figure 18 and column 15, lines 1-24).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of applying a pre-charge signal according to a black display grade as taught by Kasai in the self-luminescent display apparatus taught by the combination of Kimura, Tsuruoka et al. and Abe in order to shorten the driving time of the data lined used in the unit circuits (Kasai, column 1, lines 54-55).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 7:30 a.m. - 4:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

7 September 2010